

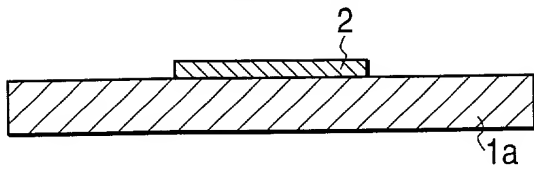
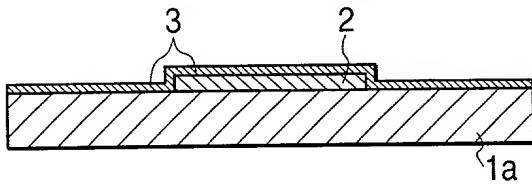
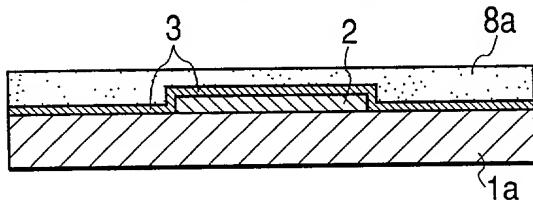
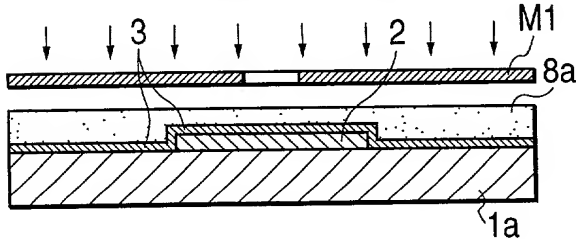
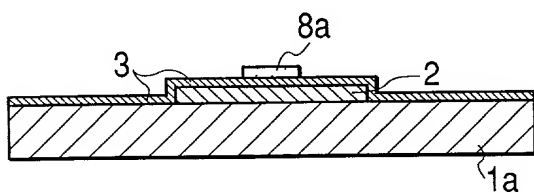
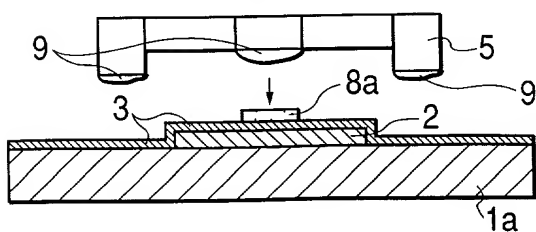
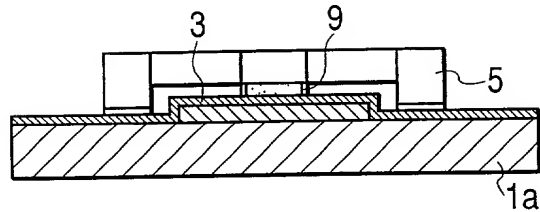
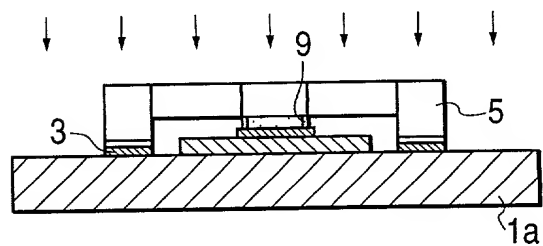
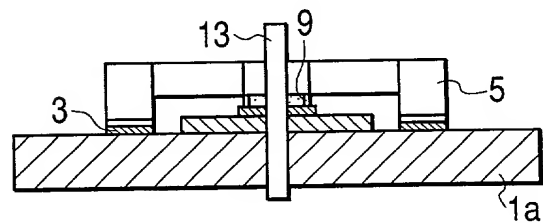
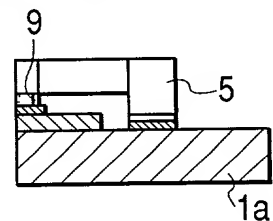
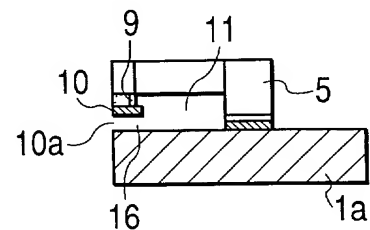
FIG. 1A**FIG. 1B****FIG. 1C****FIG. 1D****FIG. 1E****FIG. 1F****FIG. 1G****FIG. 1H****FIG. 1I****FIG. 1J****FIG. 1K**

FIG. 2

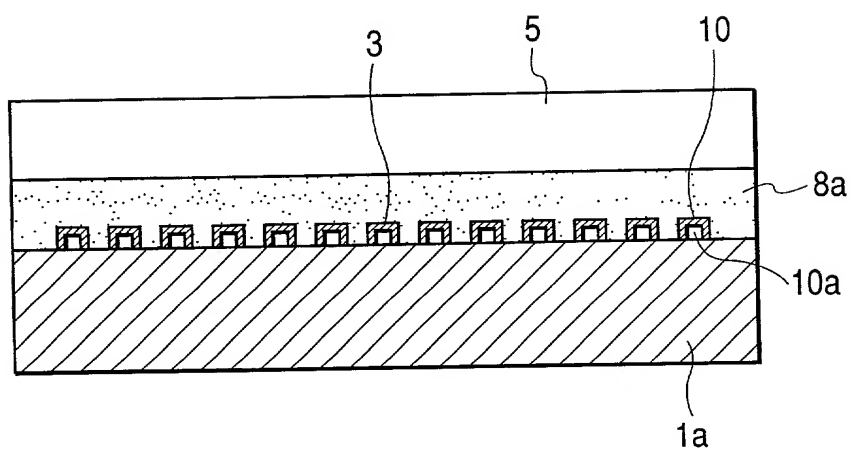


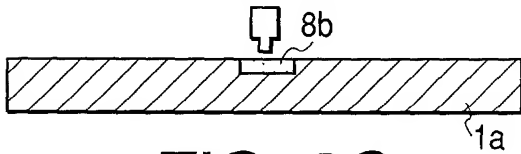
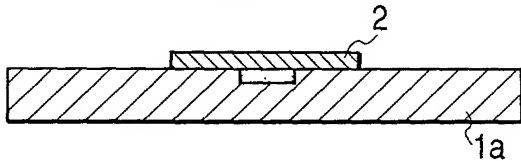
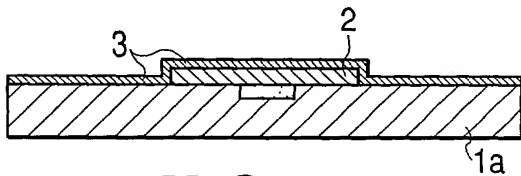
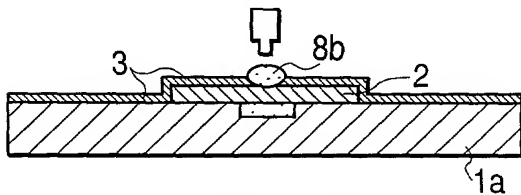
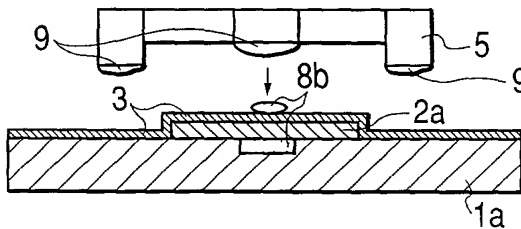
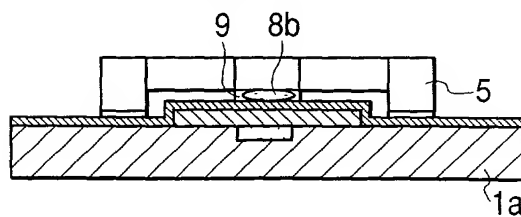
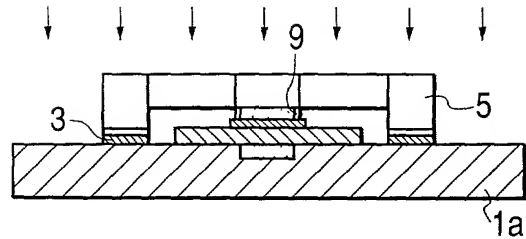
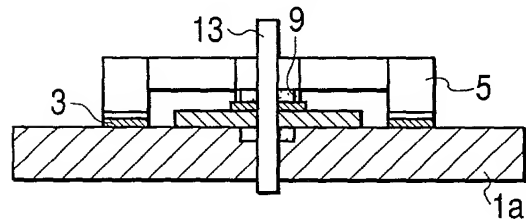
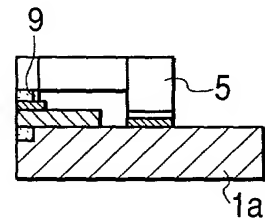
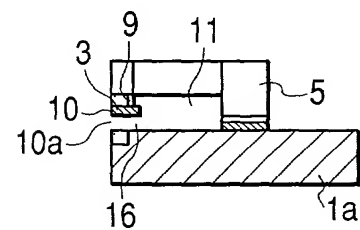
FIG. 3A**FIG. 3B****FIG. 3C****FIG. 3D****FIG. 3E****FIG. 3F****FIG. 3G****FIG. 3H****FIG. 3I****FIG. 3J****FIG. 3K**

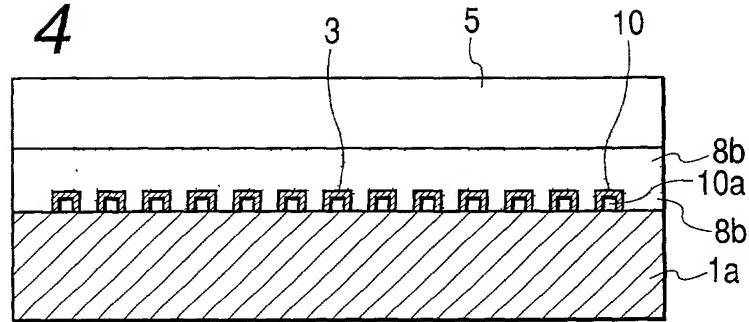
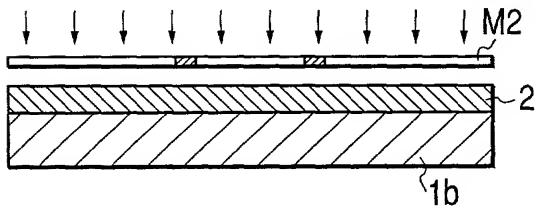
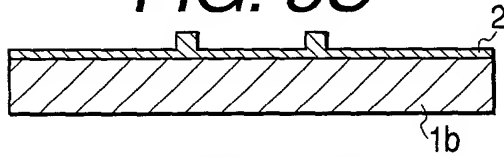
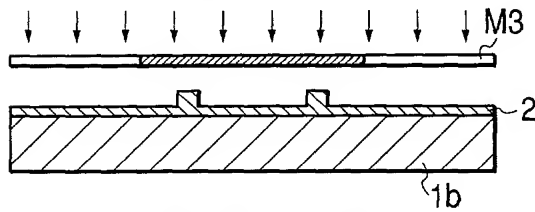
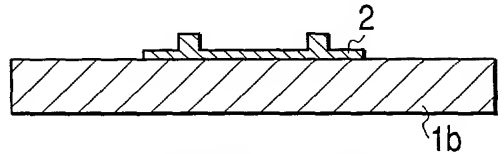
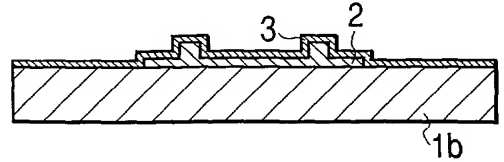
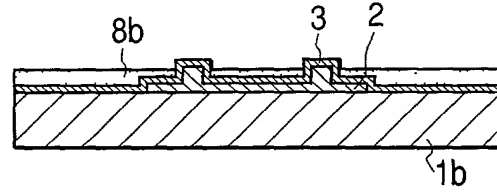
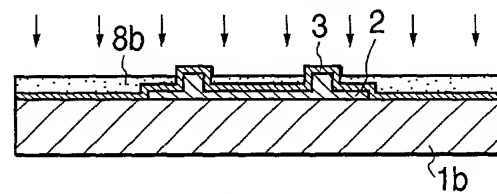
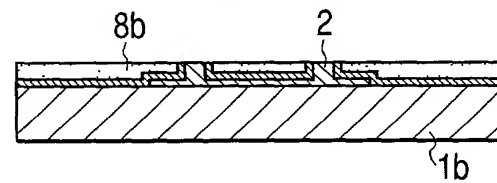
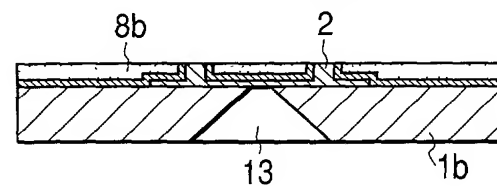
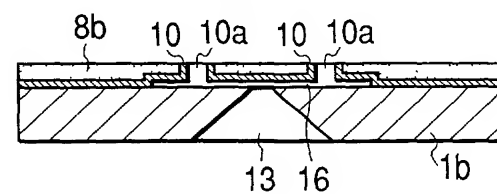
FIG. 4**FIG. 5A****FIG. 5B****FIG. 5C****FIG. 5D****FIG. 5E****FIG. 5F****FIG. 5G****FIG. 5H****FIG. 5I****FIG. 5J****FIG. 5K**

FIG. 6

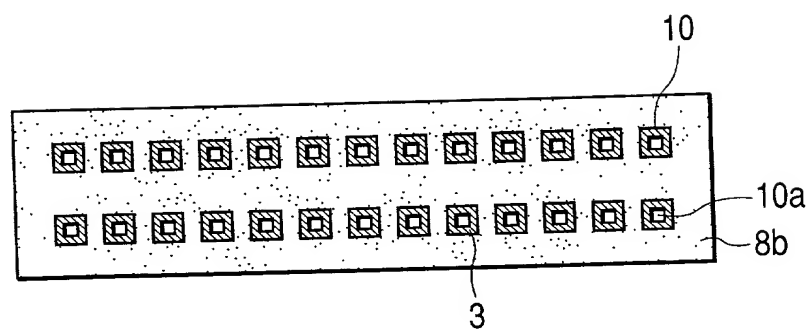


FIG. 7A

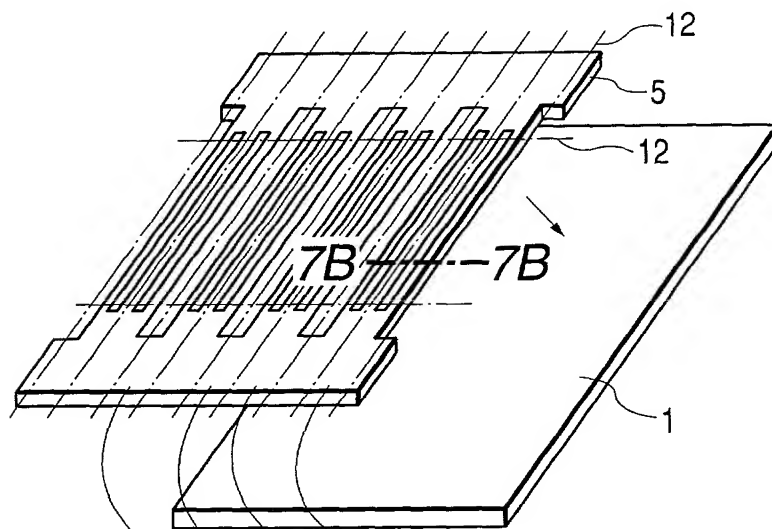


FIG. 7B

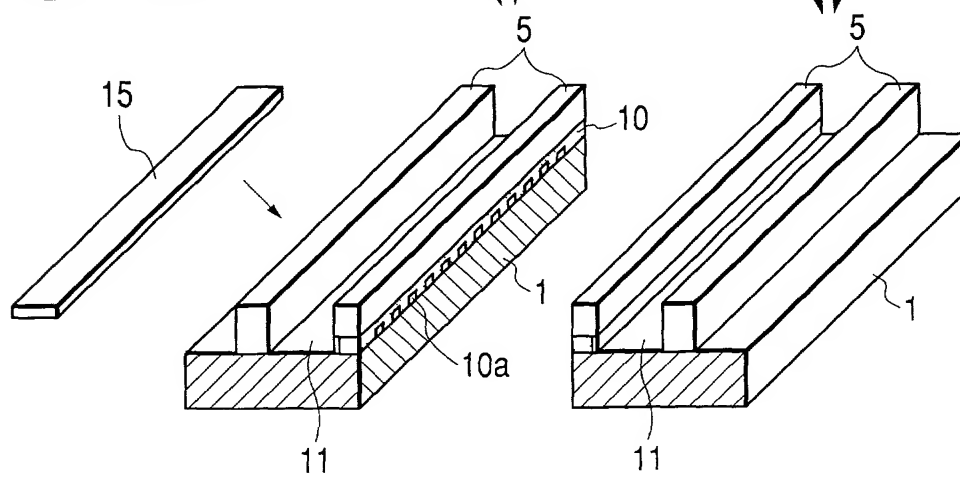


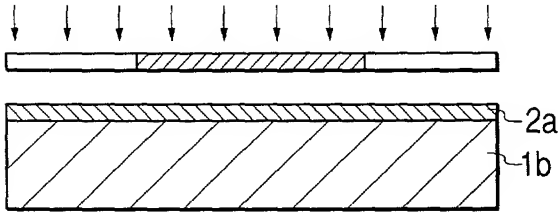
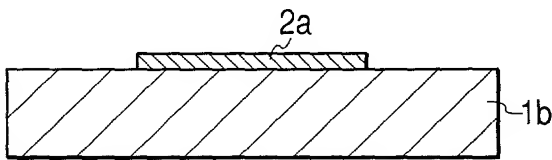
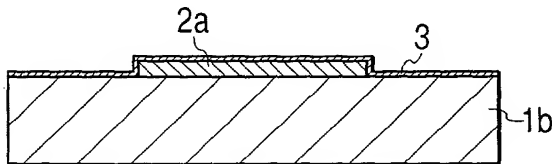
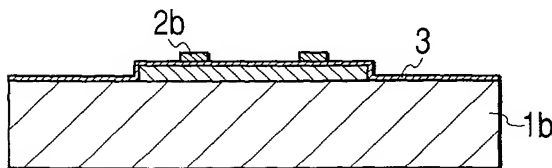
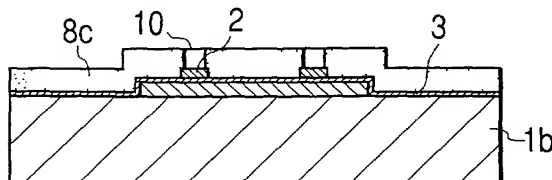
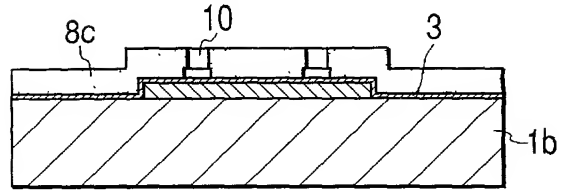
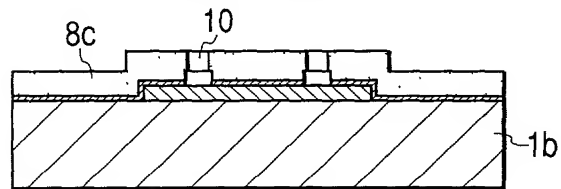
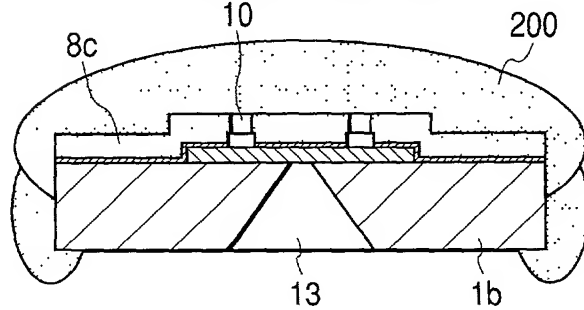
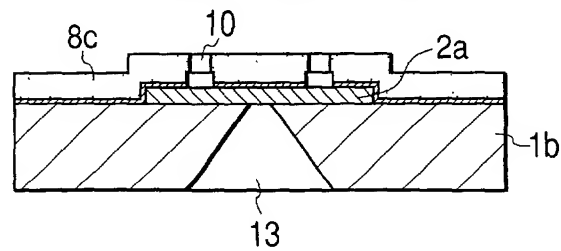
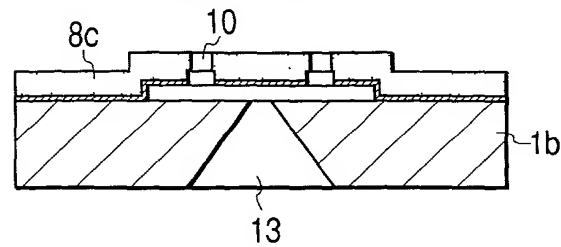
FIG. 8A1**FIG. 8A2****FIG. 8A3****FIG. 8A4****FIG. 8A5****FIG. 8A6****FIG. 8A7****FIG. 8A8****FIG. 8A9****FIG. 8A10****FIG. 8A11**

FIG. 8B

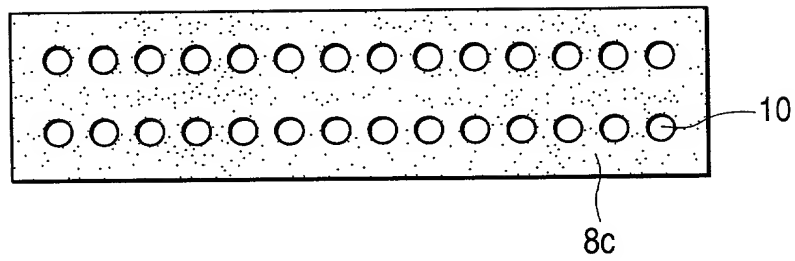


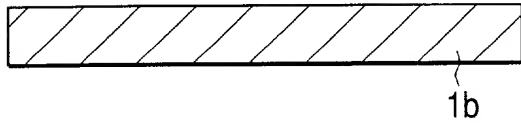
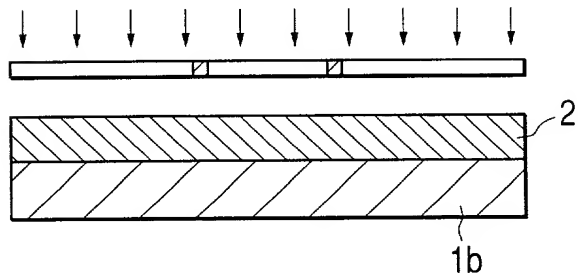
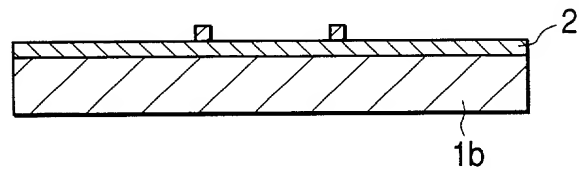
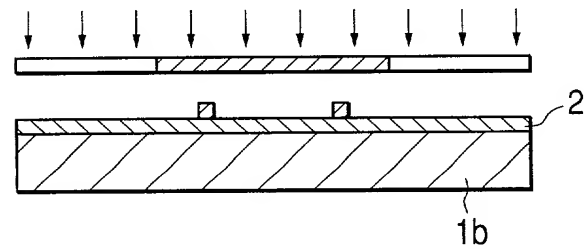
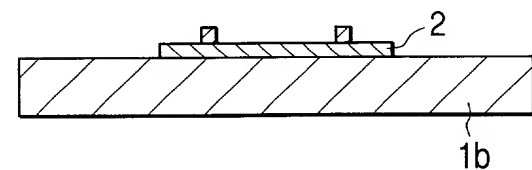
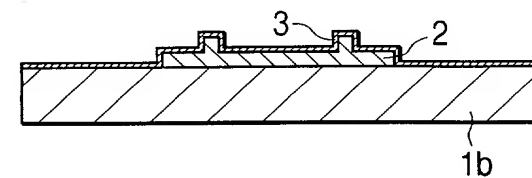
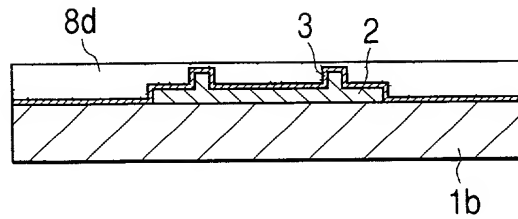
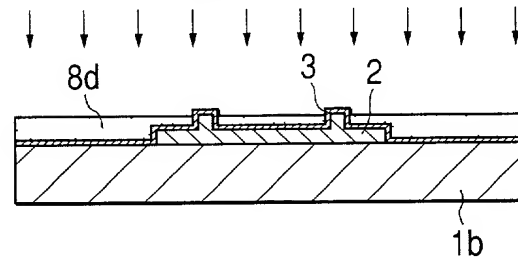
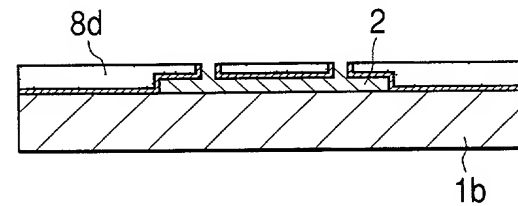
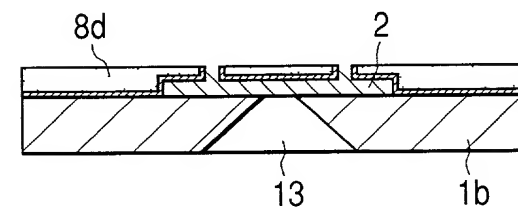
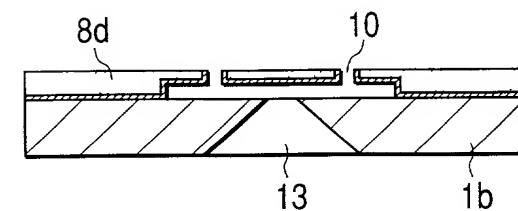
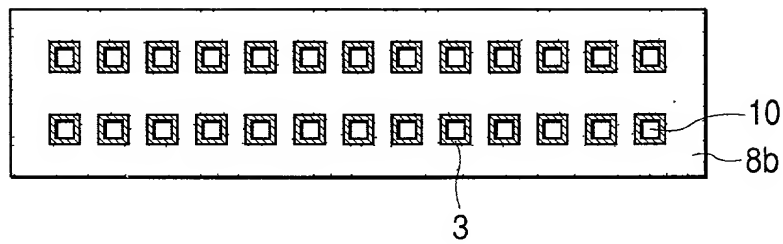
FIG. 9A1**FIG. 9A2****FIG. 9A3****FIG. 9A4****FIG. 9A5****FIG. 9A6****FIG. 9A7****FIG. 9A8****FIG. 9A9****FIG. 9A10****FIG. 9A11**

FIG. 9B



A cross-sectional view of a substrate 101. The substrate has a central opening 103. The top surface of the substrate is shown with a hatched pattern.

A cross-sectional view of a substrate 101. A conductive layer 103 is formed on the top surface of the substrate 101. A conductive pad 105 is formed on the conductive layer 103.

Figure 1 is a cross-sectional view of a semiconductor device 100. The device includes a substrate 101, a gate stack 106, a gate electrode 105, and a gate insulating layer 107. The gate stack 106 is formed on the substrate 101, and the gate electrode 105 is formed on the gate stack 106. The gate insulating layer 107 is formed on the gate electrode 105. The gate insulating layer 107 is formed on the gate electrode 105, and the gate insulating layer 107 is formed on the gate electrode 105.

This cross-sectional view shows a thin layer 107 on top of a substrate 101. The substrate 101 has a central region 105 and side regions 106. The thin layer 107 has a central region 113 and side regions 113a. Arrows indicate downward force or pressure applied to the top surface of the thin layer 107.

This diagram shows a cross-sectional view of the second embodiment of the semiconductor device. It features a substrate 101 with a base layer 106. A central layer 105 is positioned between two semiconductor regions 113. The regions 113 are covered by a layer 114, which is in turn covered by a top layer 107. The central layer 105 is shown as a thin layer between the two semiconductor regions 113.

This diagram shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate 101 with a first conductive layer 105 and a second conductive layer 106. A central region contains a gate stack 113, which includes a gate insulating layer 114 and a gate electrode 119. A second conductive layer 107 is positioned above the gate stack 113, and a second conductive layer 106 is positioned below it. A second conductive layer 105 is also shown at the bottom of the central region.